Thomas J. Rosenbauer

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Objective

To offer consulting services for organizations seeking a top notch engineer with embedded hardware, and software design expertise and a security clearance.

Qualification Summary

Proven track record of 20+ years of successful embedded product development that demonstrates proficiency in the following areas:

- Proposals
- System architecture
- Hardware design
- FPGA design
- Software design
- System integration
- DO-178/254 certification and documentation
- Trouble shooting and problem solving

Technical skills

Security Clearance

Embedded Development

- Processors: ARM, AVR, NIOS, MicroBlaze, 680x0
- Operating systems: Windows, Linux, VxWorks
- Software: network protocol stacks, TCP/IP, board support packages, device drivers, real-time applications

Hardware Design

- DO-254 compliance
- Printed circuit board: schematic capture, net list, component placement, routing, OrCAD, SPICE simulation
- Digital: FPGA, Digital Signal Processor (DSP), Video, digital filters, Microprocessor, peripherals, memory subsystems,
- Analog: Signal conditioning, A/D conversion, PLL, transient/EMI suppression
- Power Supply
- Gigabit serializers, deserializers (SERDES)
- Interfaces: 10/100/1000 Ethernet, sFPDP, PCI, SPI, USB, ARINC 717, IRIG 106, ARINC 429, 1553, CAN, wireless, custom

FPGA Design

- Devices: ArriaII, Cyclone, SmartFusion, Virtex, Apex, 20KE, 10KE, PLD
- Languages: AHDL, VHDL, Verilog
- IP integration
- System on a programmable chip (SOPC)
- Simulation, Verification, ModelSIM Testbenches

Software Design

- DO-178 compliance
- Languages: C/C++, Visual Basic
- Development Platform: Visual Studio, Eclipse
- Graphical User Interface: MFC, OpenGL

Experience

Consultant 1999 – Present
Rosenbauer Consulting, Inc. – Easton, PA

- Provided embedded software and hardware design services for Cobham in support of their SEWIP program.
- Implemented automated antenna test/calibration system with OrbitFR.
- Provided VHDL design and system integration services for L3-Telemetry East in support of the **NetDAS** product line. Design elements included an embedded MicroBlaze processor core on a Xilinx (Virtex family) FPGA.
- Provided embedded software development and system integration services for L3-Aviation Recorders in support of the **Accelerometer** program. Software effort involved algorithm development, diagnostics and calibration for production, and DO-178 certification. A patent was issued for the intellectual property created for this program.
- Provided digital design services for L3-Aviation Recorders in support of the **AV700 satellite receiver**. Design elements included a Sirius RF module, AT91RM9200 microprocessor with peripherals to support embedded Linux application, communication, audio and ARINC subsystems, and DO-160 avionic power supply. Designed product upgrade that incorporated a Z-Wave wireless remote control.
- Provided digital design services for L3-Aviation Recorders in support of the **DASU Flight Data Recorder**. Designed 16-channel **Strain Gauge module** (PC-104 form factor) with embedded Atmel AVR processor. Implemented embedded software with data acquisition and signal processing algorithms.
- Provided digital design services for L3-Telemetry East in support of the **IntelliBus program**. Employed Altera FPGAs (Cyclone II family) with embedded NIOS CPU core and custom DSP and communications subsystems. Design also included mixed-signal processing elements for data acquisition: analog signal conditioning, analog filtering, A/D converters, DMA data buffering, DSP processing, D/A converters, transducer excitation.
- Provided digital design services for L3-Telemetry East in support of the **Hot Launch program**. Employed Altera FPGAs (Cyclone family) with embedded NIOS CPU core and custom PCM and flash memory subsystems.
- Provided mixed digital and analog design services for L3-Telemetry East in support of the **SAM program**. Employed Altera FPGAs (Apex 20KE family) with embedded NIOS CPU core and custom DSP and ARINC subsystems.
- Provided digital design services for L3-Aviation Recorders in support of the **Voyage Data Recording program**. Employed Altera FPGAs (10KE family), PCI IP (Intellectual Property), ADPCM transcoders, and analog CODECs for a PCI based Audio Acquisition module.
- Provided proposal, system architecture and digital design services for L3-Telemetry East in support of the **THAAD program**. Employed Altera FPGAs (Apex 20KE family) with embedded NIOS CPU core and custom digital I/O and PCM subsystems.
- Provided digital design services for L3-Microcom in support of the **Coleman MICRODAS project**.
- Provided digital design services for L3-Microcom in support of the **MADRAS flight data recorder program**. Employed Altera FPGAs (10KE family), Actel FPGAS (MX-4) and i186 Microprocessors for data acquisition and PCM subsystems. Board designs included 8 channel ARINC429 module, 48 channel Discrete Conditioner, 32 channel Analog Multiplexer, 8 channel Frequency Module, and 8 channel Synchro/Ratiometric Module. Provided software support for DO-178 requirements.

Chief Technologist, Project Manager 1988 – 1999
Chyron Corporation – Melville, NY

- Architected and developed Chyron's Duet, a multi-channel DTV video-graphics platform. Employed advanced 3D graphics chips (GMX2000), OpenGl, embedded processors (i960RD), PC components (NLX440), 1.5 Gb/s serial digital video ASIC's, Altera CPLD's (FLEX 10K, 9K and 7K), LVDS Channel Links, CPCI/PCI bus interfaces, RTOS (VxWorks), NT4.0, Tornado, Visual Studio C/C++, SoftIce.
- Researched, proposed, and implemented a real-time graphics engine to provide special

effects for television productions. Defined the hardware and software architecture and validated the design using simulation. Directed and managed a small team of engineers as principal lead engineer for hardware and software. Provided leadership and design expertise that successfully executed the project from concept to on-air application in broadcast television. Proposed and implemented a second-generation product with enhanced functions. Made extensive use of Field Programmable Gate Arrays (FPGAs) using Hardware Description Language (HDL).

- Proposed and implemented a digital video interface for Chyron's Maxine graphics generator. The digital interface implemented 4 channels of the Serial Digital Interface (SDI), a 270Mb/sec standard requiring expertise with high-speed logic design. The board also provided a genlockable sync generator with very low jitter. This required expertise with Phase Lock Loops (PLLs) and mixed analog and digital design. The design also required several special effects and filters that demonstrated expertise with video signal processing.
- Provided advanced research and evaluation on emerging technologies, scouted potential development partners, and advised management on technical issues.
- Provided trade show support by trouble shooting prototype systems, gathering technical feedback from customers, and analyzing competitive products. Presented a technical paper at a SMPTE conference, subsequently published in the SMPTE Journal.
- Assumed project management of LIDIA II. By trouble shooting several hardware and software problems, the product was successfully put back on track, delivered to the customer, and put on-air for broadcast operations.
- Provided a networking solution for Chyron's graphics generators by implementing TCP/IP, Ethernet software drivers, and FTP applications under pSOS.
- Designed and implemented a Unix driver for Chyron's Centaur, a video interface for Silicon Graphics (SGI) workstations. Developed GUI control panel application using Motif/X Windows. Also acted as a technical liaison for Centaur application software developers such as SoftImage, Wavefront, and Alias.
- Implemented an XRAY based distributed software development environment using PC's, Unix workstations, and single board computers running pSOS, a real-time operating system (RTOS). This required the development of software drivers, command shells, and utility programs using C and assembly language.
- Used PCB (Printed Circuit Board) design tools to help develop a High Definition TV graphics system that was used for the 1992 Olympic broadcasts.

Education

New York Institute of Technology
Old Westbury, NY

- M.S., Computer Science

Lafayette College
Easton, PA

- B.S., Electrical Engineering
- Graduated with Honors and Cum Laude
- F.W. Smith Award - Excellence in Engineering Research Award for Senior Thesis
- Tau Beta Pi - National Engineering Honor Society
- Eta Kappa Nu - Electrical Engineering Honor Society

Affiliations

- College Hill Presbyterian Church, Treasurer
- Lafayette College, ECE Advisory Board member
- Pennsylvania Randonneurs, Regional Brevet Administrator of long distance bicycling events.
- IEEE, Member